Selective Vapor-Liquid-Solid Epitaxial Growth of Micro-Si Probe Electrode Arrays With On-Chip MOSFETs on Si (111) Substrates

Takeshi Kawano, Yoshiko Kato, Ryoji Tani, Hidekuni Takao, Kazuaki Sawada, and Makoto Ishida

***Abstract*—This paper reports on a fabrication technique for realizing micro-Si probe arrays with MOSFETs on the same Si substrate. Micro-Si probe arrays have been successfully fabricated on Si (111) substrates by selective vapor-liquid-solid (VLS) growth using catalytic Au dot arrays and Si_2H_6 used as the gas source for a molecular-beam-epitaxy. The Si probes can be grown at temperatures ranging from 500 °C to 700 °C. In this paper, MOSFETs were fabricated on Si (111) substrates and Au dots were placed at the drain regions of the MOSFETs in order to grow the Si probes. VLS growth at 700 °C for 2 h was carried out on these substrates. Consequently, the MOSFETs can be used in on-chip circuits for the VLS-Si probe array. The electrical characteristics of the MOSFETs were measured before and after the VLS process. After the VLS process, no changes in the MOSFET characteristics were observed due to the effects of Au-diffusion, and the results confirmed that VLS growth at a temperature of 700 °C allows fabrication of micro-Si probes without deterioration of the MOSFETs. VLS-Si probes with controlled conductance were realized. The as-grown Si probes were of high resistance, but could be changed to various conductivities by impurity diffusion.**

***Index Terms*—Au-diffusion, microelectrodes, MOSFETs, Si (111) substrate, vapor-liquid-solid (VLS).**

I. INTRODUCTION

MICROELECTRODE techniques can be applied to neural recording as well as stimulation for the study of nervous systems. It is well known that the size of a single neuron is of the order of 10^{-5} to 10^{-4} m in diameter and that millions of neurons are distributed in neuronal tissue. Recent microelectromechanical systems (MEMS) technology has enabled electrodes of a similar size to one neuron to be fabricated. In addition, high-density microelectrode arrays are useful tools for analyzing complex neural networks. In clinical applications, long-term connections with neurons for delivering neural signals to prostheses have become an important topic. Also, the incorporation of on-chip integrated circuits (ICs) with these electrode arrays to improve the performance is an important technique.

In neural recording or stimulation, microelectrodes that penetrate the neuronal tissue have been fabricated by various groups. The shape of the penetrating electrode allows the microelectrodes to reach neurons in the tissue. There are several different approaches to achieving penetrating microelectrodes. A typical MEMS-based microelectrode consists of a shank on which the microelectrode array is located. This type was first developed in 1985 [1]. The shank electrode technique was expanded to a multi-shank design with an on-chip CMOS signal processor [2]. Another type of penetrating electrode is a needle-like electrode array fabricated on a Si substrate. This type of array can be realized using a dicing process [3] and an array such as this mounted on a CMOS chip has also been proposed [4]. These penetrating electrodes have a suitable shape for reaching neurons in the neuronal tissue. However, in this technique, the electrodes need to be only a few microns in size in order to reduce the damage to neurons during electrode penetration. An array of micro-Si probe electrodes each with a few microns in diameter combined with an on-chip IC has been proposed by our group using a standard IC process followed by selective growth of vapor-liquid-solid (VLS)-Si probes [5], [6].

VLS growth using Au as a catalyst and Si_2H_6 gas at a growth temperature of 700 °C, allowed micro-Si probe growth on a Si (111) substrate with a growth rate of more than 1 μm/min [7]. To achieve an on-chip IC, MOSFETs need to be fabricated on a Si (111) substrate and Au dots have to be placed near the MOSFETs. The Au may diffuse into the channel regions of the MOSFETs during high temperature VLS growth. It has been observed that Au diffusion into MOSFETs causes changes in the threshold voltage, leakage current and mobility [8], [9]. The conductance of the as-grown Si probes is low, because VLS growth using Si_2H_6 gas is done without impurity doping. In this paper, we discuss the design of the Si probe integrated with the MOSFETs, fabrication of the MOSFETs on Si (111) substrates, the effects of Au diffusion due to VLS growth, and the potential of the MOSFETs for realizing an on-chip IC for the VLS-Si probes. A conductive-Si probe formed by phosphorous diffusion in IC-compatible conditions is also discussed.

II. VLS-SI PROBE ARRAY ON MOSFETS

Fig. 1 shows the structure of a VLS-Si probe with a MOSFET on a Si (111) substrate. The selective VLS growth is carried out after the IC process [5], [7]. The site and diameter of the probe can be controlled by the patterned Au dot. The Au dot acts as a catalyst for thermal decomposition of the gas source

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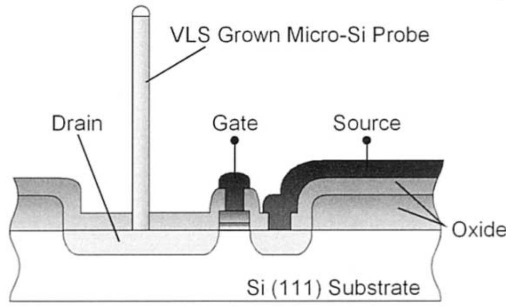

Fig. 1. Structure of a VLS-Si probe with a MOSFET on a Si (111) substrate.

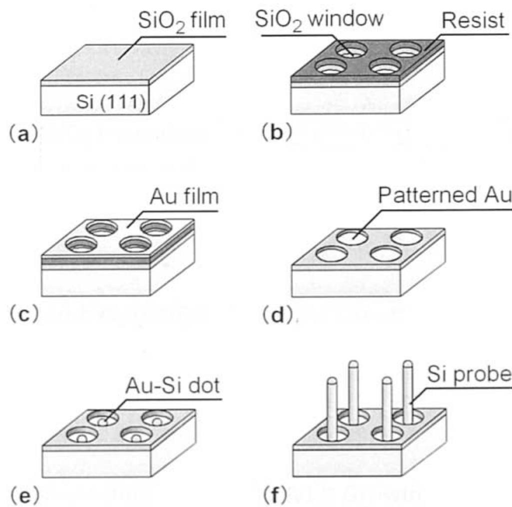

Fig. 2. Schematic diagram of the process sequence for selective vapor-liquid-solid (VLS) Si probe growth after the IC process.

molecules of Si during growth. Therefore, the deposition rate of the growth increases, and is several orders of magnitude larger than that of conventional selective Si growth. Also, the Si probes can be grown at low temperatures, because the Au acts as a catalyst at temperatures higher than the Au-Si eutectic temperature of 363 °C. Decreasing the growth temperature is very important for on-chip ICs. In addition, the Au catalyst protects the growing Si probe from crystalline defects, ensuring high stability and high quality of the Si probe. Fig. 2 shows the process sequence for selective VLS growth at predetermined probe sites. First, a 600-nm-thick SiO_2 mask was formed by CVD over the circuits, and patterned in order to open windows in the SiO_2 [Fig. 2(a) and (b)]. The diameters of the SiO_2 windows in this work were designed to be from 4 to 10 μm. A 160-nm-thick Au film was deposited by evaporation over the photoresist after etching the SiO_2 windows. The Au film on the photoresist was then removed by lift-off, and patterned Au dots were obtained at predetermined sites [Fig. 2(c) and (d)]. The substrate was introduced into the GS-MBE chamber, and annealed at 500–700 °C to form Au–Si alloy dots [Fig. 2(e)]. Then Si_2H_6 gas was introduced into the chamber at a gas pressure of 10^{-3} Pa. The Si_2H_6 gas causes the Au–Si alloy to become supersaturated with Si, resulting in precipitation of Si at the interface between the Au–Si alloy and the Si substrate. As a result, epitaxial single crystal Si probes were grown with the Au–Si alloy dot at the tip [Fig. 2(f)].

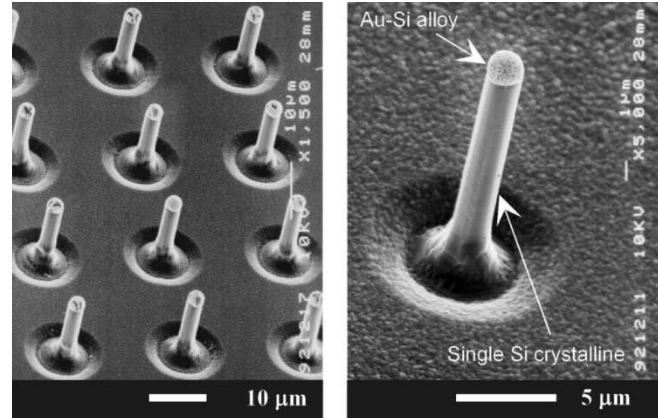

Fig. 3. SEM views of Si probes grown by selective VLS growth using a Au catalyst and Si_2H_6 gas. The VLS growth realizes micro-Si probes with a Au–Si alloy dot at the tip and a single crystalline Si body.

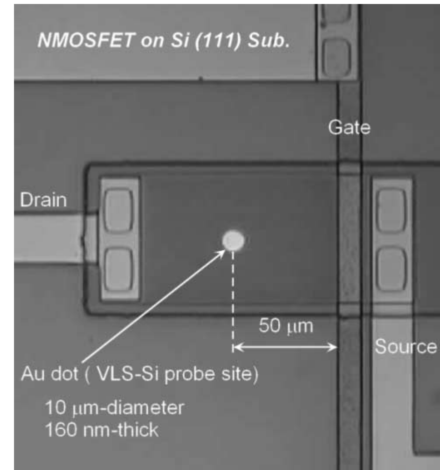

Fig. 4. Photograph showing an NMOSFET with a Au dot 10 μm-in in diameter and 160 nm thick at the VLS-Si probe site. The distance of the Au dot site was 50 μm from the gate region.

Fig. 3 shows a scanning electron microscope (SEM) view of a micro-Si probe array selectively grown at 650 °C.

III. On-Chip MOSFETs

Before the VLS growth, the on-chip MOSFETs have to be fabricated on the same Si (111) substrate. However, it is well known that Si (100) substrates are used in standard MOSFET processes, because the SiO_2/Si interface-trap density of (100) substrates is low compared to (111) substrates. The larger interface-trap density of (111) substrates causes a shift in the threshold voltages of MOSFETs. The threshold voltage, however, can be adjusted by controlling the amount of dopant in the channel region by ion-implantation. Formation of Au dots on the same surface as the MOSFETs is required in order to grow the VLS-Si probes. It was predicted that Au-diffusion into the MOSFETs would take place during growth. In this paper, the effects of Au diffusion were also investigated using NMOSFETs fabricated on a Si (111) substrate. In the design, a Au dot was placed at each of the drain regions of the MOSFETs. In the MOSFET fabrication process, W interconnection wiring was used because of the high-temperature VLS growth process.

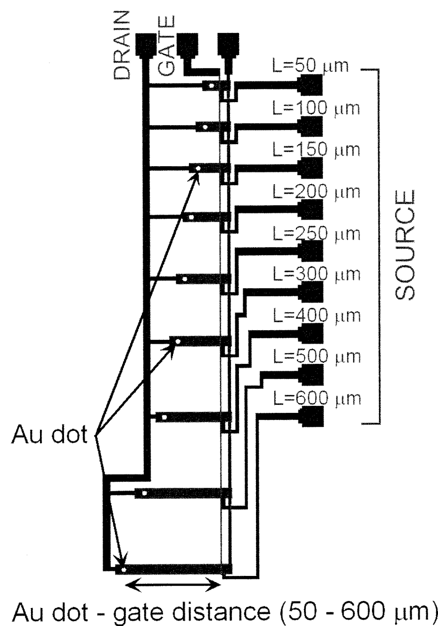

Fig. 5. Experimental NMOSFET array on a Si (111) substrate to investigate the effects of Au diffusion. The distance of the Au dot site from the gate varies from 50 to 600 μm.

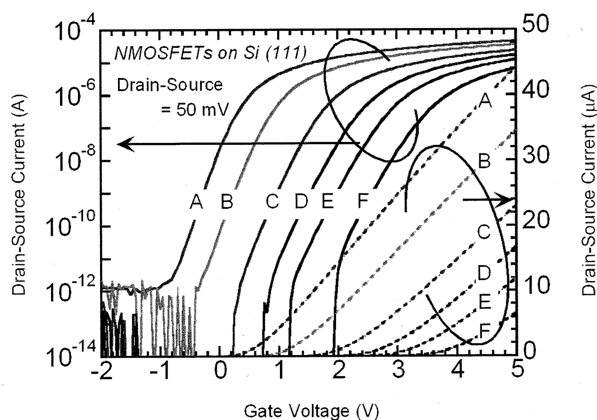

Fig. 6. I_D–V_G curves of NMOSFETs on a Si (111) substrate measured as a function of boron-doping into the channel region (A: Implanted boron-dose was 1×10^{13} cm^{-2}, B: 2×10^{13}cm^{-2}, C: 4×10^{13} cm^{-2}, D: 6×10^{13} cm^{-2}, E: 8×10^{13} cm^{-2} and F: 1×10^{14} cm^{-2}).

The Au dots were formed using the process detailed in Fig. 2. Fig. 4 shows a photograph of a fabricated NMOSFET with a Au dot at the drain, which is 50 μm from the gate. The Au dots were 10 μm in diameter and 160 nm in thickness. Fig. 5 shows the experimental NMOSFET array with a Au dot situated at various distances ranging from 50 to 600 μm from the gate to investigate the dependence of MOSFET performance on the Au-diffusion length.

Fig. 6 shows the variation of drain current I_D with gate voltage V_G of fabricated NMOSFETs with various threshold voltages. The I_D–V_G curves were plotted as a function of controlled boron doping into the Si substrate ranging from 1×10^{13} cm^{-2} (A) to 1×10^{14} cm^{-2} (F). During the measurement, a constant drain voltage of 50 mV was used. A field-effect-mobility of 450 cm^2/V $\cdot$ s and subthreshold swing S of 200 mV/decade were obtained. These characteristics are inferior to those on similar NMOSFETs on a Si (100) substrate produced in this work, which are 710 cm^2/V $\cdot$ s and 151 mV/decade, respectively. However, the leakage current between the drain and the source was found to be less than 10^{-12} A for all NMOSFETs fabricated on Si (111) substrates.

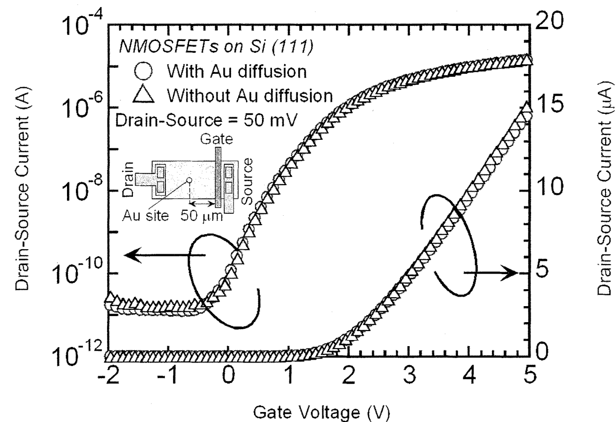

Fig. 7. I_D–V_G curves of NMOSFETs on a Si (111) substrate with and without Au-diffusion measured after a VLS growth process at 700°C for 2 h. The Au dot sites are 50 μm from the gate region of the MOSFETs.

Two types of NMOSFET on Si (111) substrates were prepared, one with Au dots and one without Au dots, and these were introduced into the GS-MBE vacuum chambe, which was maintained at a vacuum of 10^{-7} Pa. The Si substrates were heated from the backside to a temperature of 700 °C for 2 h during VLS growth. Under this growth condition, the interface-trapped charge at the gate region on the (111) substrate was increased due to thermal annealing in the vacuum chamber. This was established by measuring a shift in the threshold voltage and a high leakage current of 10^{-9} A. The increased interface-trapped charge can be neutralized by a low-temperature hydrogen anneal. Fig. 7 shows the I_D–V_G curves of a Au-diffused MOSFET with a Au dot at a distance of 50 μm from the gate (Fig. 4) after a hydrogen anneal at 460°C for 45 min. The electrical characteristics show no shift in the threshold voltage, and a lower leakage current of 10^{-11} A. Fig. 7 shows the I_D–V_G curves of the same NMOSFET without Au diffusion, and it confirms that the Au diffusion does not alter the MOSFET characteristics after VLS growth. Fig. 8(a) and (b) show the threshold voltage shift, leakage current, subthreshold swing and mobility before and after VLS growth as a function of the distance of the Au dot from the gate. These characteristics show that there is no significant dependence of the electrical characteristics on this distance.

It is known that diffused Au atoms remove majority carriers from the conduction band in n-type Si substrates or from the valence band in p-type substrates. As a result, the resistance of the substrates increases. Also the threshold-voltage shift of the MOSFETs may depend on the Au diffusion temperature due to additional Au charge [8], [9]. The diffusion length and the solid solubility of Au in Si are given as a function of the diffusion temperature and time. For VLS growth at a temperature of 700 °C for 2 h, the Au-diffusion length was estimated to be approximately 200 μm. Therefore, in the case where the Au dot is 50 μm from the gate (Fig. 4), the Au would have completely

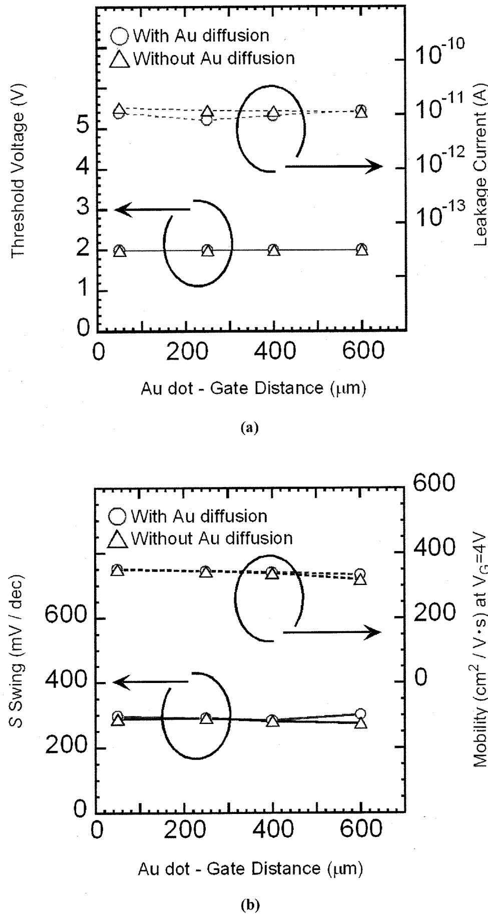

Fig. 8. Dependence of the electrical characteristics of NMOSFETs on the distance of the Au dot site from the gate before and after VLS growth at 700 °C for 2 h. (a) Threshold-voltage shift and leakage current of devices. (b) S Swing and mobility.

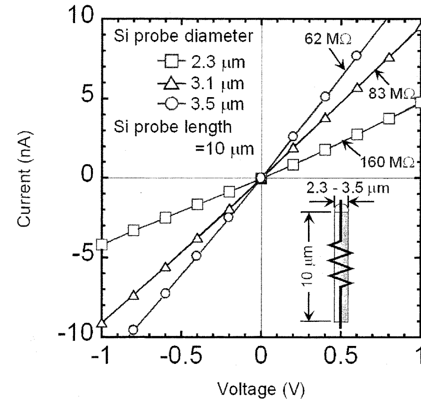

Fig. 9. I–V characteristics of as-grown VLS Si probes.

diffused into the channel region of the MOSFET. The solid solubility of the Au in the channel region was estimated to be of the order of 10^{13} cm^{-3}. However, the Au diffusion had no effect on the electrical characteristics of the MOSFETs. In this work, p-type Si (111) substrates were used with a boron doping concentration of 10^{16} cm^{-3}, which is higher than that of the solid solubility of Au under the VLS growth conditions. It was observed that the electrical characteristics of the MOSFETs were not significantly changed due to the Au diffusion, as the concentration of the diffused Au was lower than that of the doping impurity in the substrate. To achieve Au concentrations of more than 10^{16} cm^{-3} in the Si substrate, temperatures higher than 1000°C are required.

IV. Conductive-VLS Si Probe Compatibility

In VLS growth with a Au catalyst and Si_2H_6 gas, the body of the probes are single crystal Si and there is a Au-Si alloy at the tip [6]. Fig. 9 shows the current–voltage (I–V) characteristics of the as-grown Si probes measured between the tip and the base of the probes. In this measurement, tungsten microneedles mounted on x–y-z micromanipulator systems were used to contact the Si probe tip and the base. The measured I–V characteristics were linear, which indicates that the Au-Si alloy on the top of the probe forms an ohmic contact with the Si. The diameters of the probes were from 2.3 to 3.5 μm and the length of all the probes was 10-μm. The resistance of the Si probes with 3.5 μm diameter and 10-μm length was 62 MΩ, and the resistivity was of the order of 10^4 $\Omega \cdot$ cm. To obtain conducting probes for applications as microelectrodes, phosphorous diffusion was performed by introducing $POCl_3$ as a dopant source in a quartz reaction tube. In previous work [7], diffusion was done at 1100 °C, realizing heavy phosphorus doping of the Si probes. At this temperature, the resistivity of the doped-Si probes decreased to 10^{-2} $\Omega \cdot$ cm. However, in this work, a lower IC-compatible diffusion temperature should be used for the Si probes with MOSFETs. Nevertheless, it is expected that with diffusion temperatures less than 1100 °C, conductive micro-Si probes can also be realized, because the sidewalls of the Si probes can be heavily doped with phosphorous.

The temperature of the phosphorous diffusion into the Si probe was decreased to the same temperature as the VLS growth, that is, 700 °C. Fig. 10 shows the resistance of the Si probes as a function of the probe diameter after phosphorous diffusion at 700 °C for 2 h. The diameters of the doped-Si probes were from 2.3 to 3.5 μm and the length of all probes was 20 μm. The resistance of doped-Si probes of 3.5 μm diameter and 20-μm length was 6.5 MΩ, which is 1/10 the resistance of an as-grown Si probe with 3.5-μm diameter and 10-μm length. By increasing the diffusion time to more than 2 h, lower resistance probes can be realized at the same temperature of 700 °C. Fig. 10 also shows the resistances of the probes doped at 800 °C and 900 °C using the same diffusion time of 2 h. At 900 °C, a high-doped region was obtained at a depth of 0.5-μm below the surface of the probe sidewall, allowing good conductivity Si probes to be fabricated.

Fig. 11 shows a SEM view of a Si probe, grown in the drain region of an NMOSFET on a Si (111) substrate using the above-fabrication process. The Si probe was grown at 600 °C, and the probe length is sufficient to be used for neuronal tissue penetration. After being penetrated, the Au-Si alloy probe tip would be oxidized in the saline environment of the neuronal tissue. For this reason, it is necessary to apply a metal coating over the probe tips. The metal-coating process was performed with Au. First, hexamethyldisilazane (HMDS) was applied to the substrate and the Si probes by dripping liquid HMDS onto the substrate. Then, liquid resist was dripped onto the substrate until the whole surface of the substrate and all of the probes were

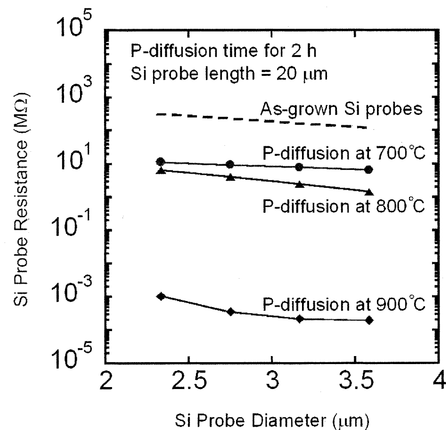

Fig. 10. Conducting properties of Si probes formed by phosphorous diffusion at 700 °C, 800 °C, and 900 °C as a function of the probe diameter.

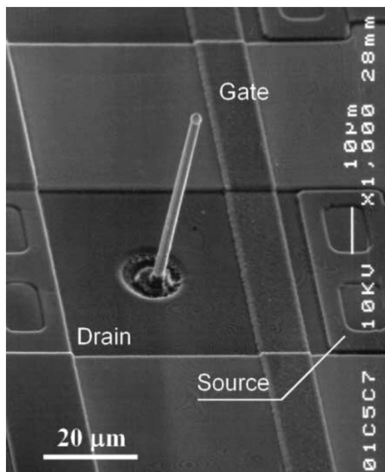

Fig. 11. SEM view of a penetrating micro-Si probe grown at the drain region of a MOSFET on a Si (111) substrate.

covered. The substrate was spun to remove excess resist using a spinner system. After the process, the remaining resist was fully cured by baking, and a resist coating over the substrate and Si probes was realized. At the probe tips, the covered resist was etched by etch-back in a plasma until the Au-Si alloy dots on the probe tips were exposed. Finally, the probe tips were covered with a layer of Au deposited by evaporation and the remaining resist along with the Au layer on top, was removed by lift-off. The impedance of the conductive-Si probe (Fig. 11) with a Au coated tip, when measured in saline solution (0.9% NaCl), was found to be of the order of 1 MΩ at 1 kHz. Using the metal-coating process, the micro-Si probe tips can be covered with any metal, such as Au, Pt, Ir, or Ti, suitable for electrodes in saline environments for realizing charge transfer during neural recoding or stimulation.

V. Conclusions

The fabrication technique for a micro-Si probe array with on-chip MOSFETs has been discussed. In this paper, Si probe arrays were grown by selective VLS growth and MOSFETs were fabricated on the same Si (111) substrate. Control of the threshold voltage of the MOSFETs was realized by ion implantation. It was expected that the MOSFETs would be affected by the Au diffusion during VLS growth of the probes; however after VLS growth at 700 °C for 2 h, the electrical characteristics of the MOSFETs showed no significant changes due to the Au diffusion. These results demonstrate the feasibility of the fabrication of VLS-Si probe arrays with on-chip MOSFETs. The Au-Si alloy on the top of the Si probe forms an ohmic contact with the Si, and conductive probes were realized by phosphorous diffusion in IC-compatible conditions.

An application of the micro-Si probes in neuroscience was proposed. Moreover, the micro-Si probe technique with on-chip IC will provide new microelectrode devices that can be used in other applications.

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